

## FIGURE 2

卷之三

TITLE: LOW LATENCY LOCK FOR MULTIPROCESSOR COMPUTER SYSTEM  
INVENTOR: Hahn Vo  
ATTY. FEE NO.: H052617.1142US0

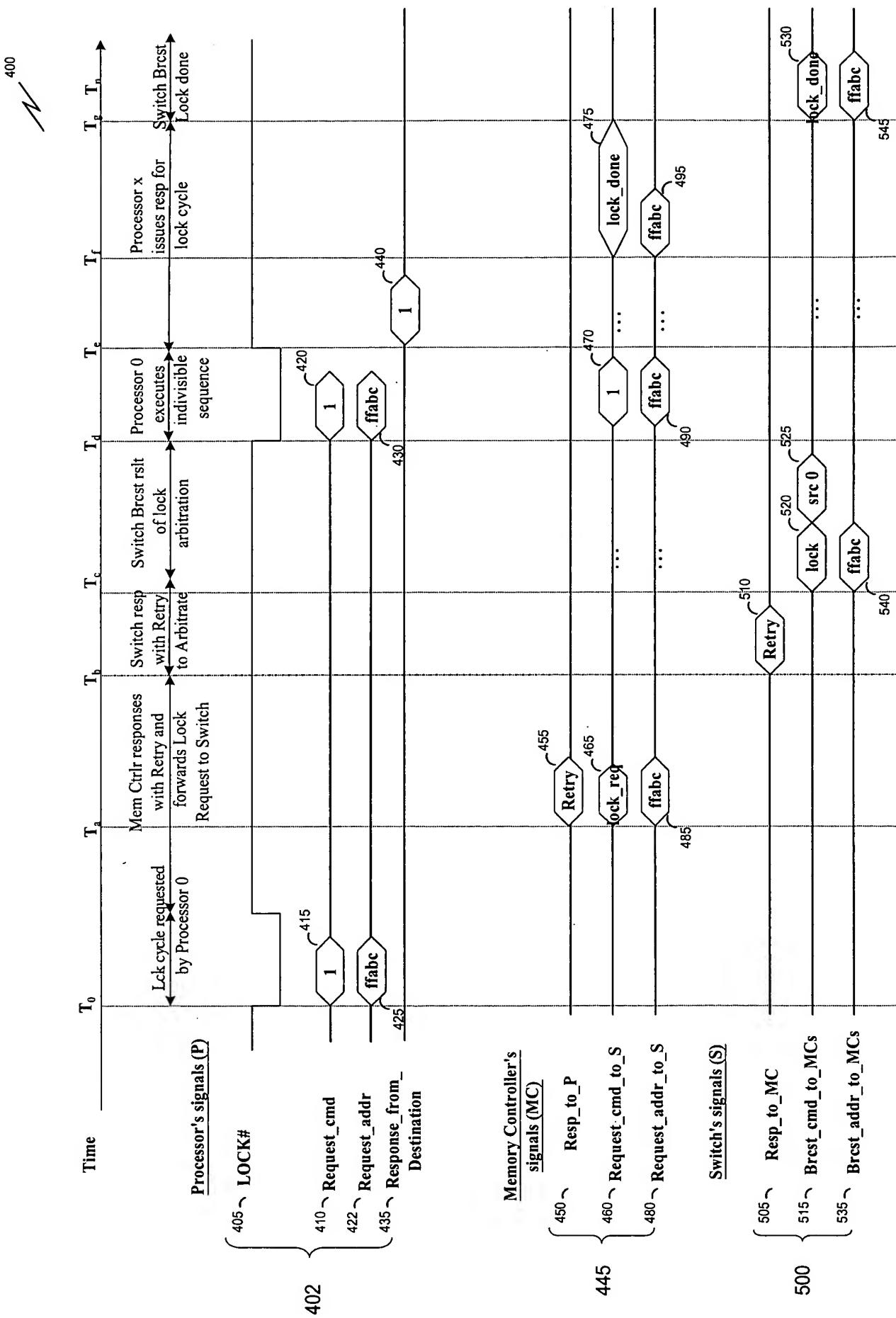
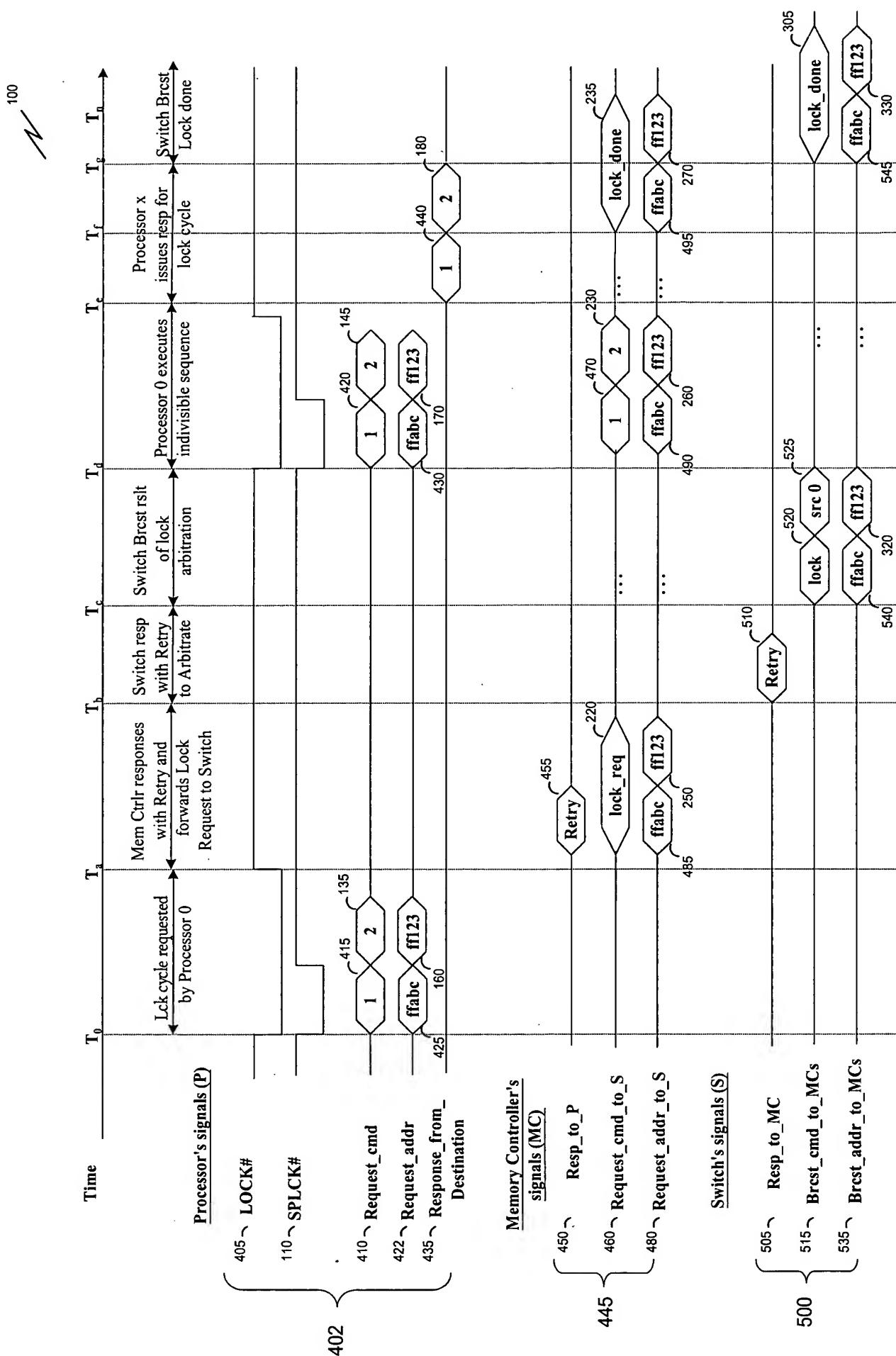


FIGURE 3

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**INVENTOR:** Hahn Vo  
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## LOCK FLOW CHART

One lock per system  
"LCK REG" "LOCK" "LOCKED" "CLOCK"

FIGURE 4

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INVENTOR: Hahn Vo  
PATENT DKT NO.: H052617.1142US0

